



6.2. SID

The SID in the 1541Ultimate is an accurate (but not perfect) implementation of the 6581/8580 sound chip in the C64. Actually, the implemented SID is a 16-voice variant of the well-known triple voice original. Eight (8) of these voices are mapped to the left output channel, and another 8 are mapped to the right channel. The register map is made such that each set of 8 voices has its own 'global' registers, such that it appears like there are two independent SID devices in the system.

6.2.1. SID mapper

The SID mapper provides a way to map the 256 registers of this 16-voice SID into two independently configurable memory (I/O) regions. Since the original SID only provides three voices, the SID mapper can work in two modes for each SID; the 3-voice mode and the 8-voice mode. In 3-voice mode, only 32 register locations are used, while in 8-voice mode 128 registers are used.

In 8-voice mode; the registers should be located on a multiple of \$80 bytes. Selecting an address that is not a multiple of \$80 bytes will result in the SID to 'snap' to the lower \$80 multiple (i.e. \$D520 becomes \$D500).

6.2.2. Memory map

In 8-voice mode; the memory map is as follows:

Offset	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
\$00	FREQ Lo 1	F7	F6	F5	F4	F3	F2	F1	F0
\$01	FREQ Hi 1	F15	F14	F13	F12	F11	F10	F9	F8
\$02	PW Lo 1	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$03	PW Hi 1	—	—	—	—	PW11	PW10	PW9	PW8
\$04	Control 1	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$05	A/D 1	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$06	S/R 1	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$07	FREQ Lo 2	F7	F6	F5	F4	F3	F2	F1	F0
\$08	FREQ Hi 2	F15	F14	F13	F12	F11	F10	F9	F8
\$09	PW Lo 2	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$0A	PW Hi 2	—	—	—	—	PW11	PW10	PW9	PW8
\$0B	Control 2	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$0C	A/D 2	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$0D	S/R 2	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$0E	FREQ Lo 3	F7	F6	F5	F4	F3	F2	F1	F0
\$0F	FREQ Hi 3	F15	F14	F13	F12	F11	F10	F9	F8
\$10	PW Lo 3	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$11	PW Hi 3	—	—	—	—	PW11	PW10	PW9	PW8



\$12	Control 3	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$13	A/D 3	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$14	S/R 3	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$15	FC Lo	–	–	–	–	–	FC2	FC1	FC0
\$16	FC Hi	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3
\$17	Res/Filt	RES3	RES2	RES1	RES0	–	FILT3	FILT2	FILT1
\$18	Mode/Vol	3OFF	HP	BP	LP	VOL3	VOL2	VOL1	VOL0
\$19-\$1F	Reserved	–	–	–	–	–	–	–	–
\$20	FREQ Lo 4	F7	F6	F5	F4	F3	F2	F1	F0
\$21	FREQ Hi 4	F15	F14	F13	F12	F11	F10	F9	F8
\$22	PW Lo 4	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$23	PW Hi 4	–	–	–	–	PW11	PW10	PW9	PW8
\$24	Control 4	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$25	A/D 4	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$26	S/R 4	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$27	FREQ Lo 5	F7	F6	F5	F4	F3	F2	F1	F0
\$28	FREQ Hi 5	F15	F14	F13	F12	F11	F10	F9	F8
\$29	PW Lo 5	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$2A	PW Hi 5	–	–	–	–	PW11	PW10	PW9	PW8
\$2B	Control 5	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$2C	A/D 5	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$2D	S/R 5	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$2E	FREQ Lo 6	F7	F6	F5	F4	F3	F2	F1	F0
\$2F	FREQ Hi 6	F15	F14	F13	F12	F11	F10	F9	F8
\$30	PW Lo 6	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$31	PW Hi 6	–	–	–	–	PW11	PW10	PW9	PW8
\$32	Control 6	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$33	A/D 6	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$34	S/R 6	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$35	FREQ Lo 7	F7	F6	F5	F4	F3	F2	F1	F0
\$36	FREQ Hi 7	F15	F14	F13	F12	F11	F10	F9	F8
\$37	PW Lo 7	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$38	PW Hi 7	–	–	–	–	PW11	PW10	PW9	PW8
\$39	Control 7	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$3A	A/D 7	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$3B	S/R 7	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$3C	FREQ Lo 8	F7	F6	F5	F4	F3	F2	F1	F0
\$3D	FREQ Hi 8	F15	F14	F13	F12	F11	F10	F9	F8
\$3E	PW Lo 8	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0
\$3F	PW Hi 8	–	–	–	–	PW11	PW10	PW9	PW8
\$40	Control 8	Noise	Pulse	Saw	Triangle	TEST	RingMod	Sync	Gate
\$41	A/D 8	ATK3	ATK2	ATK1	ATK0	DCY3	DCY2	DCY1	DCY0
\$42	S/R 8	STN3	STN2	STN1	STN0	RLS3	RLS2	RLS1	RLS0
\$43	FiltExt	FILT8	FILT7	FILT6	FILT5	FILT4	FILT3	FILT2	FILT1
\$44-\$7F	Reserved	–	–	–	–	–	–	–	–



Ring modulation and sync voice linkage is as follows:

- Voice 1 is modulated by voice 3
- Voice 2 is modulated by voice 1
- Voice 3 is modulated by voice 2
- Voice 4 is modulated by voice 8
- Voice 5 is modulated by voice 4
- Voice 6 is modulated by voice 5
- Voice 7 is modulated by voice 6
- Voice 8 is modulated by voice 7.

This SID in principle does support readback of ENV₃ and OSC₃. However; the readback path itself is currently not implemented; as it would interfere with the snooping interface. In the I/O range it could be made to work.

6.2.3. Filter

The filter curve is completely programmable through I/O registers from the Ultimate CPU into a 1024-entry lookup table (LUT); so yes the FCo bit is don't care. By default, the 6581 filter is loaded. Currently, the 8580 filter is not yet supported in the software.

6.2.4. Combined waveforms

There are two modes for combined waveforms; the 6581 mode and the 8580 mode.

In 6581 mode, the combined waveforms that are actually put on the output are sampled with the REU using a real 6581 (R1) chip. Differences in sound appearance of these waveforms make me believe that the actual output to the DAC and to OSC₃ is not the same. Also, there seems to be a frequency dependency in this. This is not emulated.

In 8580 mode, the waveforms are AND'ed together, as some resources suggest.